LIGHT-EMITTING DIODE

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Abstract

PURPOSE:To obtain an LED provided with a good light-emitting characteristic by using a wire bonding method when all electrodes for an element chip using an insulating substrate are connected to individual lead members.
CONSTITUTION:Individual chips are cut by using a dicing saw, one chip is taken out, the side of a reflection film 32 is die-bonded to a lead member 43 by using a Pb-Sn solder, electrodes for an n-type GaN layer 30 and an n-type Ga0.8In0.2N layer 41 are connected by 30mum phi Au wires 35 by using a wire bonding apparatus. Then, an i-type GaN layer electrode 27 is connected to a lead member 44 and an i-type Ga0.8In0.2N layer electrode 38 is connected to a lead member 43 respectively by 30mum phi Au wires 35 by using the wire bonding apparatus, and a manufactured light-emitting element 46 is sealed with a transparent epoxy resin. Consequently, all electrodes formed inside the same plane can be connected individually to lead members divided into the same number as the number of electrodes by using a wire bonding method. Thereby, an LED whose performance is stable can be supplied.

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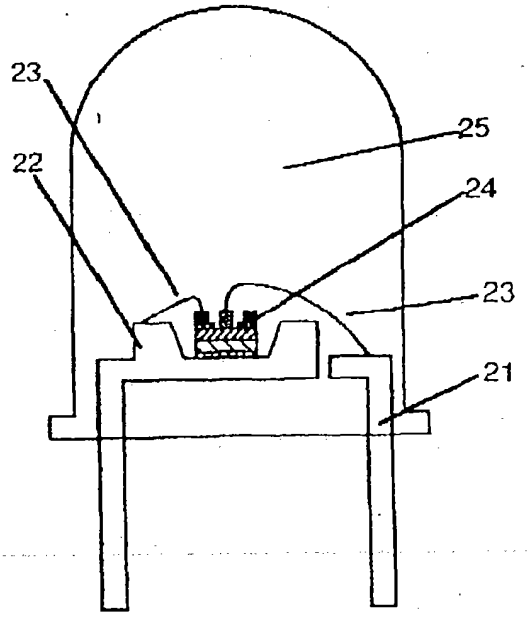
(54)【発明の名称】　発光ダイオード

(57)【要約】
【構成】　絶縁性基板上にｎ型半導体層、ｐ型およびｉ型半導体層から選ばれた２種以上の組み合わせからなる発光層を少なくとも一つ有し、かつ半導体層の所定の部位に発光層に電圧を印加するための電極を有するプレーナ構造の素子チップにおいて、電極とリード部材との接続が全てワイヤーである構造を特徴とする発光ダイオード。
【効果】　電極間の接触が少なく、発光性能に優れた、品質の安定したＬＥＤが得られる。



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【特許請求の範囲】

【請求項１】　絶縁性基板上にｎ型半導体層、ｐ型およびｉ型半導体層から選ばれた２種以上の組み合わせからなる発光層を少なくとも一つ有し、かつ半導体層の所定の部位に発光層に電圧を印加するための電極を有するプレーナ構造の素子チップにおいて、電極とリード部材との接続配線が全てワイヤーである構造を特徴とする発光ダイオード。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、絶縁性基板を用いた発光素子チップをリードフレームに実装した発光ダイオードに関する。

【０００２】

【従来の技術】従来、実用化されている発光ダイオード（ＬＥＤ）に実装されている素子チップはＧａＡｓ、ＩｎＰなどの導電性基板を用いていることから正負の電極部は素子チップの表と裏に形成されていた。従来のリードフレームに素子チップを実装し樹脂で封止したＬＥＤの断面図を図１２に示す。上述したように導電性基板を用いて作製した素子チップは表と裏に電極を有する構造をとっているため、この素子チップ２４をリードフレーム４９に接着する場合には片方の電極をリードフレームのミラー部５０にハンダあるいは導電性ペーストにより接着し、もう片方の電極はワイヤーボンディング法によってリード部材４８に接続するような構造をとっていた。　このリード部材４７、４８に素子チップを実装した後にエポキシ樹脂などで封止してＬＥＤ２５を形成していた。　近年では、透明絶縁性基板を用いたフリップチップ方式の素子チップによるＬＥＤが提案されている。（特開平４－１０６７０）この透明絶縁性基板上に発光層を形成した発光素子チップを用いて作製したＬＥＤとしては、図１３に示すような構造であり、素子チップ２４の電極１９、２０は正負の電極とも発光層側に位置し、リード部材５１、５２との接続は、ハンダあるいは導電性ペーストにより行われていた。

【０００３】

【発明が解決しようとする課題】上述したように発光素子チップに導電性基板を用いたときには、基板に電流を流すことができるので、正負の電極は基板側に１つ、発光層側に１つ形成することが可能である。リードフレームに接続する際には基板側の電極をリード部材にダイボンディングし、発光層側の電極は他のリード部材にワイヤーボンディングするという方法でＬＥＤを作製していた。しかし、透明絶縁性基板を素子チップに用いた場合には、発光層側に正負一対の電極を有するフリップチップ方式をとるため、素子チップとリード部材の接続は上述した接続方法をとることができない。このため、発光層側に形成された２種の電極をリードフレームに接続するためには、２本のリード部材の素子チップとの接続面

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は平坦にして、この平坦面に素子チップの電極面をハンダあるいは導電性ペーストにより接着する工程をとる。しかしこの方法では、同一面内に２種の電極を形成しなければならないため１ｍｍ角以下の素子チップサイズでは電極サイズは２００μｍ以下としなければならず、ハンダあるいは導電性ペーストによる接着工程において２種の電極部が接触してしまうという問題があった。また、素子チップサイズに対するハンダあるいは導電性ペーストにより接着される電極面積が広いため、より効率よく発光させるために用いられるミアンダ状、ネット状あるいはクシ状のような複雑な電極パターンを形成することはできなかった。あるいは、１つのＬＥＤから２色以上の発光を得る多色発光ダイオードを作製する場合には、３カ所以上の電極部を必要とするため電極面積はさらに小さくしなければならず、ハンダあるいは導電性ペーストによる電極とリード部材との接続は不可能であった。また、従来提案されているＬＥＤに用いる発光素子チップは透明な絶縁性基板を使用しており、発光した光を基板を通して取り出す構造のために基板による光の吸収があるため発光効率が低下するという問題点もあった。

【０００４】本発明は、前記問題点を解決して簡単に再現よく発光特性の良好なＬＥＤを提供しようとするものである。

【０００５】

【課題を解決するための手段】本発明者らは前記問題点を解決するために鋭意研究を重ねた結果、絶縁性基板を用いた素子チップの全ての電極と各リード部材とを接続する際にワイヤーボンディング法を用いることで、再現よく良好な特性を有するＬＥＤを得ることができるようになったものである。

【０００６】すなわち、本発明は絶縁性基板上にｎ型半導体層、ｐ型およびｉ型半導体層から選ばれた２種以上の組み合わせからなる発光層を少なくとも一つ有し、かつ半導体層の所定の部位に発光層に電圧を印加するための電極を有するプレーナ構造の素子チップにおいて、電極とリード部材との接続が全てワイヤーである構造を特徴とする発光ダイオードを提供するものである。

【０００７】本発明における絶縁性基板としては表面が平坦であればよく、透明でもよく不透明でもよい。絶縁性基板として代表的なものとしては、サファイア（Al_2O_3）、石英（SiO_2）、酸化マグネシウム（ＭｇＯ）、チタン酸ストロンチウム（$SrTiO_3$）、フッ化カルシウム（CaF_2）、フッ化マグネシウム（MgF_2）、酸化チタン（TiO_2）などがある。しかし、基板上に直接形成する半導体薄膜の格子定数がこの絶縁性基板の格子定数に極力合ったものを用いるのがよい。この絶縁性基板と基板上に直接形成する半導体薄膜との格子不整合は１０％以下とするのが好ましく、さらに好ましくは５％以下とするのがよい。このために該透

明絶縁性基板を所定の角度だけオフしたものを使用することも好ましいものである。例えばＧａＮの場合はサファイアＲ面を９．２°オフした基板を用いることが好ましいものとなる。また絶縁性基板と半導体薄膜との格子不整合が非常に大きい場合には、この絶縁性基板と半導体薄膜との間にバッファ層を設けてもよい。バッファ層としてはアモルファス状の物質、例えばＡｌＮ、ＧａＮ、Ｓｉ、ＳｉＣなど、あるいは単結晶物質として、例えばＡｌＮ、ＺｎＯ、ＳｉＣ等を設けることができる。

【０００８】本発明において絶縁性基板上に発光層を形成する方法としては、ＭＢＥ（Ｍｏｌｅｃｕｌａｒ Ｂｅａｍ Ｅｐｉｔａｘｙ）法、ＣＢＥ（ＣｈｅｍｉｃａｌＢｅａｍ Ｅｐｉｔａｘｙ）法、ＭＯＭＢＥ（Ｍｅｔａｌ Ｏｒｇａｎｉｃ ＭＢＥ）法、ＣＶＤ（Ｃｈｅｍｉｃａｌ Ｖａｐｏｕｒ Ｄｅｐｏｓｉｔｉｏｎ）法、ＭＯＣＶＤ（Ｍｅｔａｌ Ｏｒｇａｎｉｃ ＣＶＤ）法等の半導体成長装置を用いることができる。上記した薄膜作製方法により絶縁性基板上に発光層を形成する。この発光層はＭＩＳ構造、ｐｎ接合を有するシングルヘテロ構造およびダブルヘテロ構造、あるいは量子井戸構造あるいは超格子構造のいずれであってもよい。

【０００９】本発明における発光層とは、ｎ型半導体層、ｐ型およびｉ型半導体層から選ばれた２種以上の組み合わせからなる発光層のことである。また、これらの発光層を形成する半導体は、ＩＩＩ－Ｖ族化合物半導体、ＩＩ－ＶＩ族化合物半導体のどちらでもよいが、ＩＩＩ－Ｖ族化合物半導体であるＧａＮ系半導体は絶縁性基板であるサファイア、CaF_2、ＭｇＯ等に結晶性の良好な薄膜の成長が可能であり特に好ましいものである。

【００１０】本発明での発光素子チップは絶縁性基板を用いるために発光層側の同一平面内に正負一対の電極を形成する必要があり、発光層のエッチングを行わなければならない。この発光素子チップ作製のために行うエッチング方法としては発光層の種類により、ウエットエッチング法、ドライエッチング法のどちらを用いてもよい。エッチング後に熱処理を行うことも好ましいことであり、この熱処理を行うことによりエッチングにより受けた膜質の劣化を回復することができ、界面抵抗を下げて低電圧で発光に必要な電流を得ることができる。熱処理を行う装置としては管状炉、ランプアニール炉等の雰囲気を制御できる炉であればよい。

【００１１】本発明における発光素子チップの電極形成方法としては、ＭＢＥ法、真空蒸着法、電子ビーム蒸着法、スパッタ法等がある。電極材料としてはｎ型半導体とｐ型あるいはｉ型半導体それぞれにオーミック接触が得られるものが好ましく、金属単体でもよく、２種以上の金属を混合して合金化したものを用いてもよい。このオーミック接触を得るための条件はｎ型半導体側の電極としては半導体の仕事関数よりも小さな仕事関数を有する金属がよく、ｐ型半導体側の電極としては半導体の仕事関数よりも大きな仕事関数を有する金属を用いるのがよい。例えば、ＩＩＩ－Ｖ族化合物半導体であるＧａＮの場合には、ｎ型ＧａＮ層にはＡｌ、Ｉｎ、Ｔｉ、Ｐｂ、Ｓｂ、Ｎｂ、Ｚｒ、Ｍｎ等を電極に用いることがよく、ｉ型あるいはｐ型ＧａＮ層にはＡｕ、Ｐｔ、Ｇｅ、Ａｓ、Ｉｒ、Ｒｅ、Ｒｈ、Ｐｄ、Ｎｉ、Ｗ等を電極に用いることで良好なオーミック接触が得られる。また、このオーミック電極形成後に素子チップをリード部材に接着する際に、接着性を向上させるためや、電極部の耐熱性を向上するためにオーミック電極上にＮｉ、Ｔｉ、Ａｕ、Ｗ等の金属を積層することも好ましい。

【００１２】電極形成後にAr、N_2、Ｈｅ等の不活性ガス流中あるいは該半導体の構成元素を含むガス流中で半導体の分解温度以下で熱処理することも好ましく、これにより電極と半導体との界面抵抗を下げることが可能になり、良好なダイオード特性を得ることができる。本発明におけるＬＥＤは電極側から光を取り出す構造をとるため電極形状を工夫することが好ましい。発光した光を電極側から取り出すために該ｐ型あるいはｉ型半導体層の表面を覆う電極面積は５０％以下、好ましくは４０％以下、さらに好ましくは３０％以下とすることである。そのために、電極はｐ型あるいはｉ型半導体層の表面上にパターンを形成することが必要で、パターンの例としては図４に示すネット状、図５に示すクシ状、図６に示すミアンダ状とすることができるが、さらにはこれらのパターンの組合せや渦状、島状等があるが、特にこれらに限定されるものではない。電極の幅と電極間の距離はｐ型あるいはｉ型半導体層の電気抵抗や印加する電圧の大きさにより変えればよく、電極の幅を狭くして、電極間の距離を小さくすれば、光の取り出し効率が向上する。電極の幅をサブミクロン程度とし、かつ電極間もサブミクロン程度の間隔とすることによりｐ型あるいはｉ型半導体層の表面に均一に電圧を印加するとともに光の取り出し効率も大きくすることができる。

【００１３】また、本発明においては、基板上の発光層が形成されていない面上に図１１に示すような少なくとも一種の金属反射層を設けることも好ましいものとなる。この金属層はｎ型半導体層およびｐ型あるいはｉ型半導体層を組み合わせてなる発光層において発光して基板を通して出てくる光を反射して電極側から取り出すことを可能とするものである。これにより、発光素子の光の取り出し効率を高めることができる。金属反射層として使われる材料としてはＡｌ、Ｉｎ、Ｃｕ、Ａｇ、Ｐｔ、Ｉｒ、Ｐｄ、Ｒｈ、Ｗ、Ｍｏ、Ｔｉ、Ｎｉ等の金属の単体あるいはそれらの合金がある。金属反射層は、一層だけでもよいが、リードフレームに実装するときの耐ハンダ性、耐熱性や耐ボンディング性を向上せしめるためにＮｉ、Ｗ、Ｍｏ等の高融点の金属を積層した構造とすることも好ましいものとなる。

【００１４】本発明におけるリードフレームの形状は素子チップをリード部材に固定するための接続部と、素子チップのそれぞれの部位に電圧を印加するための各電極と他のリード部材をワイヤーによってそれぞれ接続できる構造であればよく発光素子チップの電極形状により変えることができる。リードフレームは発光を有効に集光するためにミラー面を設けることが望ましい。

【００１５】本発明における発光素子チップをリード部材にダイボンディングを行う際の接着の材料としては、一般的に使われているものが使用できる。例えばＡｕ－Ｓｉ、Ｐｂ－Ｓｎ合金系ハンダや、このハンダに少量のＢｉ、Ｓｂ、Ａｇ、Ｃｄ、Ｚｎ、Ｉｎ等の金属を添加したもの、ＢｉにＮａ、Ｔｌ、Ｃｄ、Ｓｎ、Ｐｂ等を添加し合金化したもの、ＩｎにＺｎ、Ｃｄ、Ｓｎ、Ｂｉ等を添加し合金化したもの、ＧａにＡｇ、Ｚｎ、Ｓｎ、Ｉｎ等を添加し合金化したもの、Ａｕ、Ａｌ、Ｉｎ、Ａｇ等の金属あるいはＡｇ、Ａｕ、Ｃｕ等を含んだ導電性ペーストがある。素子チップとリード部材とを接着する方法としては、従来のダイボンディング装置を用いた方法がある。即ち、接着層を素子チップの該電極部、もしくはリード部材の素子チップの接着面に蒸着法、塗布法あるいはメッキ法等により形成した後、該電極部と該リード部材を密着させながらリード部材を接着材料の融点以上に加熱して接着を行う。

【００１６】また本発明における発光素子チップの電極部とリード部材を配線する際にはワイヤーボンダー法を用いることが特徴である。ダイボンディング法により素子チップをリード部材に固定した後に、ワイヤーボンディング装置にセットして加熱および、あるいは超音波を印加することにより電極部とリード部材とを接続する。このとき用いるワイヤーの材料としては、Ａｕ、Ａｇ、Ｃｕ、Ａｌ等の金属、Ａｕ－Ｓｉ、Ａｌ－Ｓｉ、Ａｌ－Ｍｇ、Ａｌ－Ｓｉ－Ｍｇ、Ａｌ－Ｎｉ等の合金があり、どの材料を使用するかは発光素子チップの電極部の材料やワイヤーボンディングの作業性を考慮して選べばよい。なかでも、ＡｕやＡｌ－Ｓｉが作業性がよいということで好ましい。ワイヤーの太さは、発光素子チップの電極部の大きやワイヤーボンディングの作業性を考慮して選べばよく、通常は２０～３００μｍφである。また、ワイヤーの酸化を防ぐために、不活性ガス中でワイヤーボンディングを行うことも好ましい方法である。

【００１７】本発明における封止材料としては発光素子チップの発光波長範囲での光透過率が８０％以上の透光性材料を使用することが好ましい。この透光性材料としては、メタクリル系樹脂、エポキシ系樹脂、ポリカーボネート系樹脂、ポリスチレン系樹脂、ポレオレフィン系樹脂あるは低融点ガラスの少なくとも一種を使用することができる。封止方法としては、たとえば所望形状の金型にこれらの透光性材料の原料または加熱溶融体を注形して金型内で固化させる方法を用いることができる。この固化の方法として、モノマーやオリゴマーの熱または光による重合固化、加熱溶融体では冷却固化、化学反応等を挙げることができる。この透光性材料には必要があれば、色調調整や視感度補正のための色素、顔料、蛍光体などを、樹脂の安定化のための酸化防止剤、安定剤、成形加工のための潤滑剤、滑剤を添加することも可能である。

【００１８】以上説明した各方法を用いて作製したＬＥＤの例を図３に示すが、これに限定されるものではない。素子チップ２４は、絶縁基板上にｎ型半導体層、ｐ型およびｉ型半導体から選ばれた２種以上の組み合わせからなる発光層を少なくとも一つ有し、かつそれぞれの半導体層の所定の部位に、発光層に電圧を印加するための電極を有するブレーナ構造の素子チップである。この素子チップの基板面あるいはリード部材２２の接着面に蒸着法でハンダを蒸着した後、リード部材２２の接着面に素子チップ２４を載せハンダの融点以上に加熱して接着する。その後、各電極とそれぞれのリード部材とをワイヤーボンディング法を用いて金線により接続する。その後、透光性材料により封止してＬＥＤ２５を作製する。

【００１９】以下、一例として絶縁性基板としてＡｌ$_2$Ｏ$_3$を使用してＭＢＥ法を用いてＧａＮ薄膜を成膜しＬＥＤを作製する方法について説明するが、とくにこれに限定されるものではない。装置としては、図１に示すような真空容器１内に、蒸発用ルツボ（クヌードセンセル）２、３および４、ガスセル７、基板加熱ホルダー５を備えたガスソースＭＢＥ装置を使用した。

【００２０】蒸発用ルツボ２にはＧａ金属を入れ、基板面において10^{13}～10^{19}／ｃｍ^2・ｓｅｃになる温度に加熱した。アンモニアの導入にはガス導入管８を用い、アンモニアをガスセル７内から基板６に直接吹き付けるようにした。アンモニアの導入量は基板表面において10^{16}～10^{20}／ｃｍ^2・ｓｅｃになるように供給した。蒸発用ルツボ３にはＩｎ、Ａｌ等を入れ、所定の組成の化合物半導体、および所定のキャリア密度を有する半導体となるように温度および時間を制御して成膜を行なう。蒸発用ルツボ４にはＭｇ、Ｚｎ、Ｂｅ、Ｓｂ、Ｓｉ、Ｇｅ、Ｃ、Ｓｎ、Ｈｇ、Ａｓ、Ｐ等を入れ、所定の供給量になるように温度および供給時間を制御することによりドーピングを行ない、ｎ型およびｉ型あるいはｐ型半導体層を成膜する。

【００２１】基板６にはサファイアＲ面を使用し、２００～９００℃に加熱した。サファイアＲ面基板は、オフ角が０．８度以下のものが好ましい。まず、基板６を真空容器１内で７５０℃で加熱した後、各ルツボを所定の成長温度に設定し、まず蒸発用ルツボ３を開き、０．１～３０オングストローム／ｓｅｃの成長速度で０．０５～２μｍの厚みのｎ型ＧａＮ薄膜を作製する。さらにその後、Ｚｎをチャージした蒸発用ルツボ４のシャッター

を開き、0．1～30オングストローム／secの成長速度で0．01～1μmの厚みでi型あるいはp型GaN薄膜を成膜して発光層を形成する。この成膜時には常にガスセルを加熱し基板表面にアンモニアを供給する。

【0022】以上のような方法で成膜した発光層を有するGaN薄膜を用いてLEDを作製する工程を図2（a）から図2（h）にしたがって説明する。真空蒸着法を用いてAl_2O_3側に金属反射膜17を蒸着する（a）。GaN薄膜表面にレジストを塗布する。レジストの膜厚はエッチングしたいGaN薄膜の厚みによって変えればよく0．1～3μmとするのが好ましい。スピンコーターの条件は2500rpm、30secである。塗布後に90℃に加熱されたクリーンオーブン内で30分間プレベークする（b）。その後、素子パターン形成用マスクを用いてUV露光・現像を行った（c）。Arをガスとして用いてイオンミリング法によりi層あるいはp層のGaN薄膜14を除去する（d）。イオンミリング終了後、アセトンを用いてレジストを除去する。

【0023】なお、各工程でのイオンミリングを行う時間はエッチングを行う膜厚によって決めることができる。以上の工程の後、管状炉内に試料をセットしてアンモニアを雰囲気として500℃で30分間熱処理した。熱処理後、再度レジストを塗布し、プレベークを行い、続いてn層電極形成用マスクを用いてUV露光・現像を行った後（e）、真空蒸着法によりn型GaN層15の電極としてAlを3000オングストロームの厚さに蒸着し、リフトオフにより電極パターン19を形成した（f）。ついで再度レジストを塗布し、プレベークを行い、i層電極形成用マスクを用いてUV露光・現像を行った後（g）、真空蒸着法によりp型あるいはi型GaN層14の電極としてAuを3000オングストロームの厚さに蒸着し、リフトオフにより電極パターン20を形成した（h）。その後、Ar流中で300℃、1時間の加熱処理を行った。

【0024】以上のようにして作製した発光素子チップの金属反射膜をハンダによりリード部材22に接着し、n型GaN層、i型GaN層の電極をワイヤーボンダー装置を用いて30μmφAu線23でそれぞれリード部材21、リード部材22にボンディングした。その後、発光素子チップを透明エポキシ樹脂によりモールディングを施し、図3に示す様な5mmφLED25を作製した。

【0025】

【実施例】以下、実施例によりさらに詳細に説明する。

【0026】

【実施例1】絶縁性基板としてAl_2O_3R面を使用し、MBE法によりGaN薄膜を成膜し、ミアンダ状の電極構造を有する素子チップを用いてLEDを作製した例について説明する。図1に示すような真空容器1内に、蒸発用ルツボ2、4、ガスセル7、および基板加熱ホルダー5、さらにガスセル7にガスを供給するためのガス導入管8を備えたMBE装置を用いた。

【0027】蒸発用ルツボ2にはGa金属を入れ、1050℃に加熱した。ガスとしてはアンモニアを使用し、ガス導入管8を通してガスセル7に5cc／minの速度で供給した。アンモニアガスは基板6に直接供給するような構造とした。基板6としては、オフ角が0．5度のサファイアR面を使用する。真空容器内の圧力は、成膜時において2×10^{-5}Torrであった。

【0028】まず、基板6を900℃で30分間加熱し、ついで750℃の温度に保持し成膜を行う。成膜はアンモニアを300℃に加熱したガスセル7から供給しながらGaのルツボのシャッターを開けて行い、1．5オングストローム／secの成膜速度で膜厚0．5μmのn型GaN薄膜を作製した。さらにMgをチャージして300℃に保たれた蒸発用ルツボ4のシャッターを開けMgドープのGaN薄膜を1．5オングストローム／secの成膜速度で膜厚0．05μmの厚さで成膜して発光層を形成した。この作製した薄膜のRHEEDパターンはストリーク状で結晶性および平坦性が良好であり、抵抗を測定したところ、10MΩ以上の抵抗があり絶縁状態であった。

【0029】発光層が形成されている基板面の反対面に真空蒸着法を用いて2×10^{-6}Torrの真空中でAlを3000オングストロームの厚みで蒸着し反射膜を形成した。続いて発光層上にスピンコーターを用いて2500rpm、30secの条件でレジストを塗布し、90℃のクリーンオーブン中で30分間プレベークした。ベーク後、素子パターン形成用のマスクを用いてUV露光し、現像した。続いて、加速電圧500V、圧力2×10^{-4}Torrの条件のArで15分間イオンミリングを行い素子パターン形成を行った。その後、アセトンを用いてレジストを除去した。次に、再度スピンコーターを用いて2500rpm、30secの条件でレジストを塗布し、90℃のクリーンオーブン中で30分間プレベークした。ベーク後、i層除去用のマスクを用いてUV露光し、現像した。続いて、加速電圧500V、圧力2×10^{-4}Torrの条件のAr雰囲気中で1分間イオンミリングを行い不必要なi層を除去した。その後、アセトンでレジストを除去した。次いで、管状炉にセットして10cc／minのアンモニアガス流中で500℃、30分間の熱処理を行った。さらに、スピンコーターを用いて2500rpm、30secの条件でレジストを塗布し、90℃のクリーンオーブン中で30分間プレベークした。ベーク後、n型GaN層の電極形成用のマスクを用いてUV露光し、現像した。続いて、真空蒸着機に装着し2×10^{-6}Torrの真空中でAl金属を0．2μmの厚さで真空蒸着した。その後、アセトンでリフトオフして電極パターンを形成した。ついで、i型

ＧａＮ層の電極形成用のマスクを用いてＵＶ露光し、現像した。続いて、真空蒸着機に装着し２×１０$^{-6}$Ｔｏｒｒの真空中でＡｕ金属を０．２μｍの厚さで真空蒸着した。その後、アセトンでリフトオフして電極パターンを形成した。この作製した発光素子をＡｒ流中で３００℃で１時間加熱処理を行い、ミアンダ状の電極構造を有する素子チップを完成させた。作製した素子チップの側面図および上面図を図７（ａ）、（ｂ）に示した。

【００３０】各チップのカッティングはダイシングソーを用いて行った。１素子チップは０．５ｍｍ×０．５ｍｍとした。このうちの１チップを取り出し反射膜側をＡｇペーストによりリード部材にダイボンディングした。さらにｎ型ＧａＮ層電極、ｉ型ＧａＮ層電極とそれぞれのリード部材とをワイヤーボンディング装置を用いて３０μｍφＡｕ線で接続した。上記の方法で作製した発光素子を透明エポキシ樹脂で封止して図８に示すようなＬＥＤを作製した。

【００３１】同様の方法で１００個のＬＥＤを作製したところ、９９個のＬＥＤで発光が確認された。このＬＥＤの発光強度を測定したところ８Ｖ，２０ｍＡで６０ｍｃｄであり、青色の発光が観測された。

【００３２】

【比較例１】実施例１と同様の方法によりＡｌ$_2$Ｏ$_3$基板上に成膜した発光層を有するＧａＮ薄膜を用いて素子化を行った。素子作製過程も実施例１と同様の方法により行い、ｎ型ＧａＮ層、ｉ型ＧａＮ層の両電極ともＡｇペーストにより、リード部材にダイボンディングを行った後、透明エポキシ樹脂で封止してＬＥＤを作製した。同様の方法で１００個のＬＥＤを作製したところ、Ａｇペーストにより正負の電極がつながってしまい、９個のＬＥＤでしか発光するものは得られなかった。

【００３３】

【実施例２】絶縁性基板としてＡｌ$_2$Ｏ$_3$Ｒ面を使用し、ＭＢＥ法によりＧａ$_{1-x}$Ｉｎ$_x$Ｎ薄膜を成膜し２色発光のＬＥＤを作製した例について説明する。図２に示すような真空容器１内に、蒸発用ルツボ２、３、４、ガスセル７、および基板加熱ホルダー５、さらにガスセル７にガスを供給するためのガス導入管８を備えたＭＢＥ装置を用いた。

【００３４】蒸発用ルツボ２にはＧａ金属を入れ、１０２０℃に加熱し、蒸着用ルツボ３にはＩｎ金属を入れ１０００℃に加熱した。ガスとしてはアンモニアを使用し、ガス導入管８を通してガスセル７に５ｃｃ／ｍｉｎの速度で供給した。アンモニアガスは基板６に直接供給するような構造とした。基板６としては、オフ角が０．５度のサファイアＲ面を使用する。

【００３５】真空容器内の圧力は、成膜時において２×１０$^{-6}$Ｔｏｒｒであった。まず、基板６を９００℃で３０分間加熱し、ついで７００℃の温度に保持し成膜を行う。成膜はアンモニアを３００℃に加熱したガスセル７から供給しながらＧａとＩｎのルツボのシャッターを開けて行い、１．５オングストローム／ｓｅｃの成膜速度で膜厚０．５μｍのｎ型Ｇａ$_{0.8}$Ｉｎ$_{0.2}$Ｎ薄膜を作製した。さらにＭｇをチャージして３００℃に保たれた蒸発用ルツボ４のシャッターを開けＭｇをドーピングしたｉ型Ｇａ$_{0.8}$Ｉｎ$_{0.2}$Ｎ薄膜を１．５オングストローム／ｓｅｃの成膜速度で膜厚０．０５μｍの厚さで成膜して第１の発光層を形成した。次に基板温度を７５０℃に上げて３０分間温度を安定させた後、Ｇａのルツボのシャッターを開けて１．５オングストローム／ｓｅｃの成長速度で膜厚０．５μｍのｎ型ＧａＮ薄膜を成長し、さらにその上に蒸着ルツボ２および４のシャッターを開けてＭｇをドーピングしたｉ型ＧａＮ薄膜を１．５オングストローム／ｓｅｃの成長速度で膜厚０．０５μｍの厚さで成膜して第２の発光層を形成した。

【００３６】発光層が形成されている基板面の反対面に真空蒸着法を用いて２×１０$^{-6}$Ｔｏｒｒの真空中でＡｌを３０００オングストロームの厚さで蒸着し反射膜を形成した。続いて、発光層上にスピンコーターを用いて２５００ｒｐｍ、３０ｓｅｃの条件でレジストを塗布し、９０℃のクリーンオーブン中で３０分間プレベークした。ベーク後、素子パターン形成用のマスクを用いてＵＶ露光し、現像した。続いて、加速電圧５００Ｖ、圧力２×１０$^{-4}$Ｔｏｒｒの条件のＡｒで２５分間イオンミリングを行い素子パターン形成を行った。その後、アセトンを用いてレジストを除去した。次に、再度スピンコーターを用いて２５００ｒｐｍ、３０ｓｅｃの条件でレジストを塗布し、９０℃のクリーンオーブン中で３０分間プレベークした。ベーク後、フォトマスクを用いてＵＶ露光し、現像した。続いて、加速電圧５００Ｖ、圧力２×１０$^{-4}$Ｔｏｒｒの条件のＡｒ雰囲気中で１５分間イオンミリングを行い不必要なｉ型ＧａＮ層、ｎ型ＧａＮ層、ｉ型Ｇａ$_{0.8}$Ｉｎ$_{0.2}$Ｎ層を除去した。次に、再度スピンコーターを用いて２５００ｒｐｍ、３０ｓｅｃの条件でレジストを塗布し、９０℃のクリーンオーブン中で３０分間プレベークした。ベーク後、フォトマスクを用いてＵＶ露光し、現像した。ついで、加速電圧５００Ｖ、圧力２×１０$^{-4}$Ｔｏｒｒの条件のＡｒ雰囲気中で１３分間イオンミリングを行い不必要なｉ型ＧａＮ層、ｎ型ＧａＮ層を除去した。さらに再度スピンコーターを用いて２５００ｒｐｍ、３０ｓｅｃの条件でレジストを塗布し、９０℃のクリーンオーブン中で３０分間プレベークした。ベーク後、フォトマスクを用いてＵＶ露光し、現像した。続いて、イオンミリングを用い不必要なｉ型ＧａＮ層を除去した。その後、アセトンでレジストを除去した。ついで、管状炉にセットして１０ｃｃ／ｍｉｎのアンモニアガス流中で５００℃、３０分間の熱処理を行った。さらに、スピンコーターを用いて２５００ｒｐｍ、３０ｓｅｃの条件でレジストを塗布し、９０℃のクリーンオーブン中で３０分間プレベークした。ベーク

後、n型GaN層およびn型$Ga_{0.8}In_{0.2}$N層の電極形成用のマスクを用いてUV露光し、現像した。続いて、真空蒸着機に装着し2×10^{-6}Torrの真空中でAl金属を0．2μmの厚さで真空蒸着した。その後、アセトンでリフトオフして電極パターンを形成した。ついで、i型GaN層およびi型$Ga_{0.8}In_{0.2}$N層の電極形成用のマスクを用いてUV露光し、現像した。続いて、真空蒸着機に装着し2×10^{-6}Torrの真空中でAu金属を0．2μmの厚さで真空蒸着した。その後、アセトンでリフトオフして電極パターンを形成した。この作製した発光素子をAr流中で300℃で1時間加熱処理を行い、素子チップの構造を完成させた。作製した素子チップの側面図および上面図を図9（a）、（b）に示す。

【0037】各チップのカッティングはダイシングソーを用いて行った。1素子チップは1mm×1mmとした。このうちの1チップを取り出し反射膜側をPb－Snハンダでリード部材にダイボンディングした。その後n型GaN層およびn型$Ga_{0.8}In_{0.2}$N層の電極をワイヤーボンディング装置を用いて30μmφAu線で接続した。さらにi型GaN層電極とリード部材、i型$Ga_{0.8}In_{0.2}$N層電極とリード部材とをワイヤーボンディング装置を用いて30μmφAu線で接続した。上記の方法で作製した発光素子を透明エポキシ樹脂で封止して、図10に示すようなLEDを作製した。

【0038】同様の方法で100個のLEDを作製したところ、95個のLEDで発光が確認された。このLEDの発光強度を測定したところリード部材66とリード部材67では10V，18mAで40mcdの青色の発光が、リード部材66とリード部材68では、8V、20mAで60mcdの緑色の発光が観測された。

【0039】

【発明の効果】本発明は絶縁性基板上に発光層を形成したプレーナ型の素子チップ構造において、同一平面内に形成された全ての電極を該電極数と同じ数に分割したリード部材にワイヤーボンディング法によりワイヤーでおのおの接続することで、安定した性能のLEDを供給することが可能になる。

【図面の簡単な説明】

【図1】　薄膜作製に用いたMBE装置の概略図である。

【図2】　（a）～（h）　LEDの作製工程を示した断面図である。

【図3】　本発明による方法で作製したLEDの断面図である。

【図4】　ネット状電極を形成した発光素子の上面図である。

【図5】　クシ状電極を形成した発光素子の上面図である。

【図6】　ミアンダ状電極を形成した発光素子の上面図である。

【図7】　（a）　実施例1で作製した素子チップの断面図である。

（b）　実施例1で作製した素子チップの上面図である。

【図8】　実施例1で作製したLEDの断面図である。

【図9】　（a）　実施例2で作製した素子チップの断面図である。

（b）　実施例2で作製した素子チップの上面図である。

【図10】　実施例2で作製したLEDの断面図である。

【図11】　発光層の形成されていない側の基板面に金属層が形成された構造からなる発光素子の断面図である。

【図12】　従来の方法で作製されたLEDの断面図である。

【図13】　従来の方法で作製されたフリップチップ方式のLEDの断面図である。

【符号の説明】

1　真空容器
2　蒸発用ルツボ
3　蒸発用ルツボ
4　蒸発用ルツボ
5　基板加熱ホルダー
6　基板
7　ガスセル
8　ガス導入管
9　流量調節バルブ
10　クライオパネル
11　コールドトラップ
12　油拡散ポンプ
13　油回転ポンプ
14　p型あるいはi型半導体層
15　n型半導体層
16　絶縁性基板
17　金属反射膜
18　レジスト
19　n型半導体層電極
20　p型あるいはi型半導体層電極
21　リード部材（1）
22　リード部材（2）
23　金属ワイヤー
24　素子チップ
25　LED
26　電極
27　i型GaN層電極
28　n型GaN層電極
29　i型GaN層
30　n型GaN層

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31　サファイア基板
32　Al反射膜
33　リード部材（3）
34　リード部材（4）
35　Auワイヤー
36　GaN発光素子チップ
37　GaNMIS型LED
38　i型$Ga_{0.8}In_{0.2}$N層電極
39　n型GaN層およびn型$Ga_{0.8}In_{0.2}$N層電極
40　i型$Ga_{0.8}In_{0.2}$N層
41　n型$Ga_{0.8}In_{0.2}$N層

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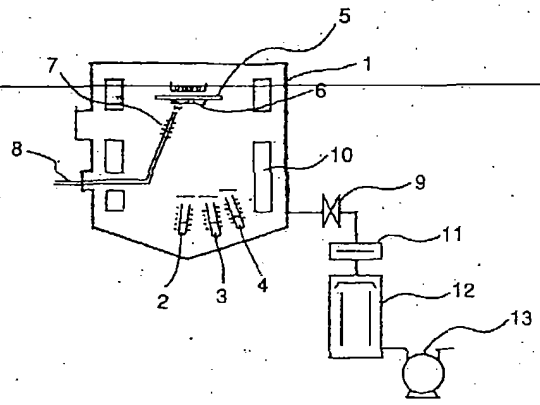
＊42　リード部材（5）
43　リード部材（6）
44　リード部材（7）
45　GaN、$Ga_{0.8}In_{0.2}$N発光素子チップ
46　2色発光LED
47　リード部材（8）
48　リード部材（9）
49　リードフレーム
50　ミラー面
51　リード部材（10）
52　リード部材（11）

【図1】



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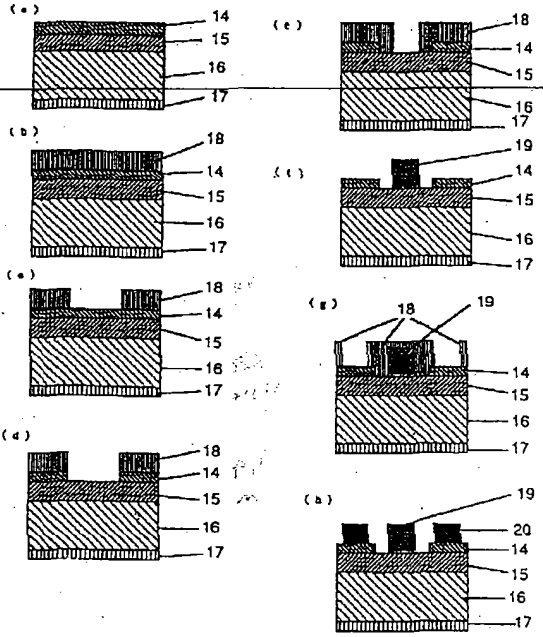

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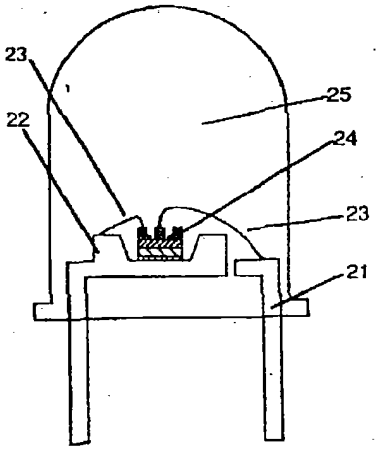

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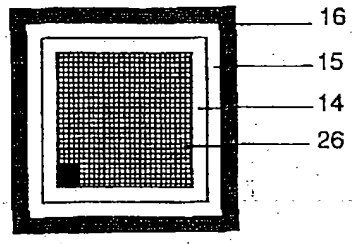

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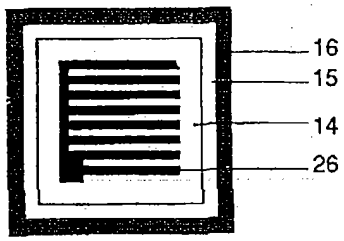
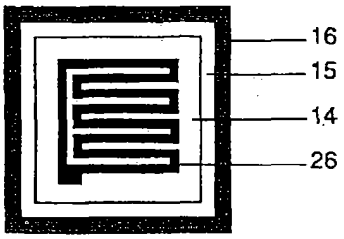


【図６】



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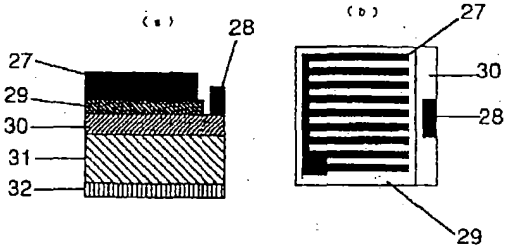

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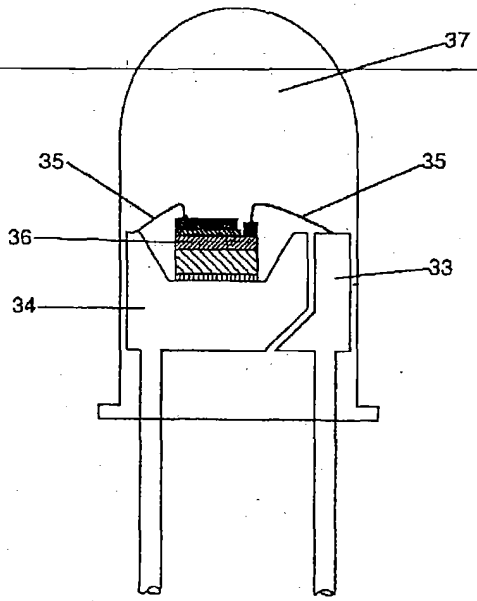
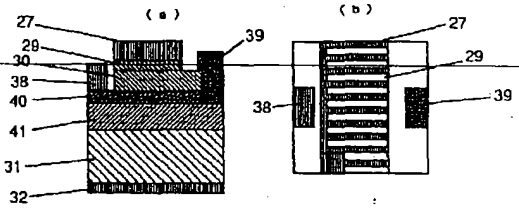
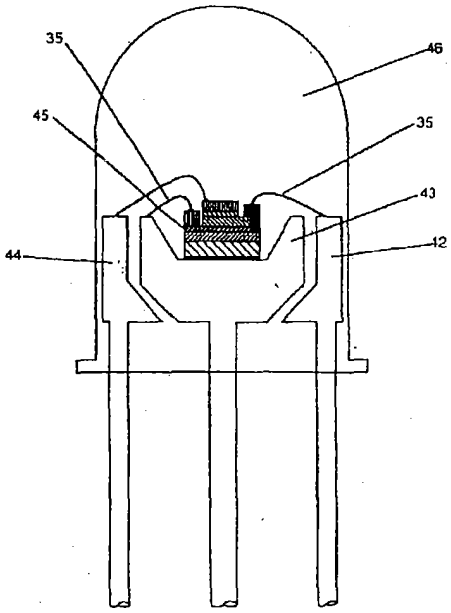


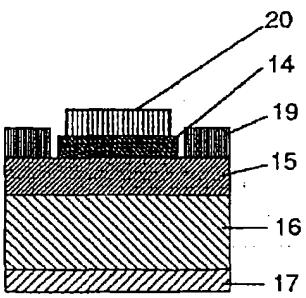
【図９】



【図１０】



【図１１】



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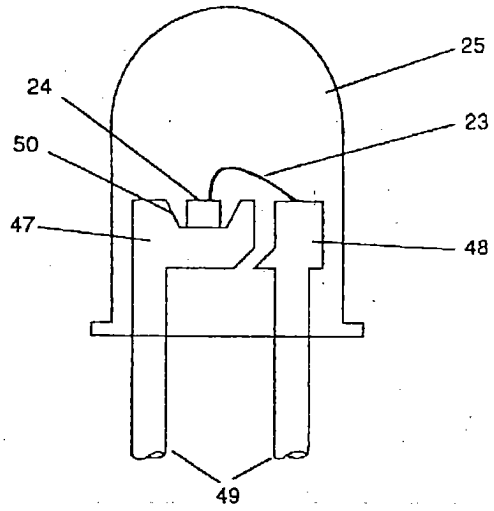
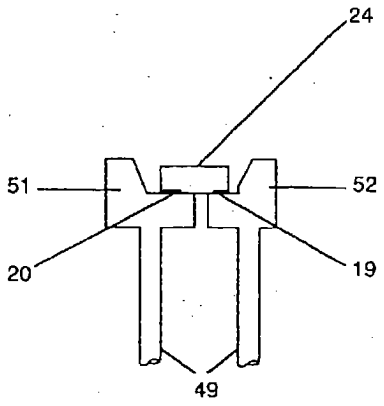


【図13】



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PATENT ABSTRACTS OF JAPAN

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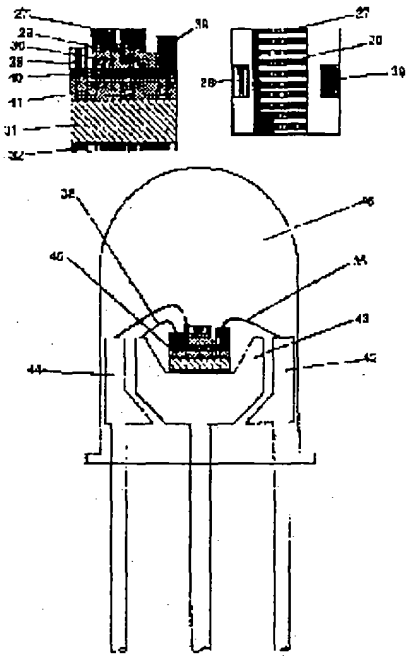
(72)Inventor : GOTOU HIROMASA
IMAI HIDEAKI

(54) LIGHT-EMITTING DIODE

(57)Abstract:
PURPOSE: To obtain an LED provided with a good light-emitting characteristic by using a wire bonding method when all electrodes for an element chip using an insulating substrate are connected to individual lead members.
CONSTITUTION: Individual chips are cut by using a dicing saw, one chip is taken out, the side of a reflection film 32 is die-bonded to a lead member 43 by using a Pb-Sn solder, electrodes for an n-type GaN layer 30 and an n-type Ga0.8In0.2N layer 41 are connected by 30 μm ϕ Au wires 35 by using a wire bonding apparatus. Then, an i-type GaN layer electrode 27 is connected to a lead member 44 and an i-type Ga0.8In0.2N layer electrode 38 is connected to a lead member 43 respectively by 30 μm ϕ Au wires 35 by using the wire bonding apparatus, and a manufactured light-emitting element 46 is sealed with a transparent epoxy resin. Consequently, all electrodes formed inside the same plane can be connected individually to lead members divided into the same number as the number of electrodes by using a wire bonding method. Thereby, an LED whose performance is stable can be supplied.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] Light emitting diode characterized by the structure where all connection wiring with an electrode and a lead member is wires, in the element chip of the planar structure which has an electrode for having at least one luminous layer which consists of two or more sorts of combination chosen from the n-type-semiconductor layer, p type, and the i-type-semiconductor layer on the insulating substrate, and impressing voltage to the predetermined part of a semiconductor layer at a luminous layer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the light emitting diode which mounted the light-emitting-device chip which used the insulating substrate in the leadframe.
[0002]
[Description of the Prior Art] Since the element chip conventionally mounted in the light emitting diode (Light Emitting Diode) put in practical use used conductive substrates, such as GaAs and InP, the polar zone of positive/negative was formed in the table and the reverse side of an element chip. The cross section of Light Emitting Diode which mounted the element chip in the conventional leadframe and was closed by the resin is shown in drawing 12 . the case where this element chip 24 is pasted up on a leadframe 49 since the element chip produced using the conductive substrate has taken the structure of having an electrode on a table and the reverse side as mentioned above -- one of the two's electrode -- the mirror section 50 of a leadframe -- a pewter or a conductive paste -- pasting up -- already -- one of the two's electrode -- the wire-bonding method -- a lead -- structure which is connected to a member 48 was taken this lead -- after mounting an element chip in members 47 and 48, it closed by the epoxy resin etc. and Light Emitting Diode25 was formed In recent years, Light Emitting Diode by the element chip of the flip chip method which used the transparent insulation substrate is proposed. (JP,4-10670,A) structure as shown in drawing 13 as a Light Emitting Diode produced using the light-emitting-device chip in which the luminous layer was formed on this transparent insulation substrate -- it is -- the electrodes 19 and 20 of the element chip 24 -- the electrode of positive/negative -- a luminous layer side -- being located -- a lead -- connection with members 51 and 52 was made with a pewter or a conductive paste
[0003]
[Problem(s) to be Solved by the Invention] Since current can be passed to a substrate when a conductive substrate is used for a light-emitting-device chip, as mentioned above, the electrode of positive/negative can be formed in a substrate side at one one and luminous layer side. Carrying out die bonding of the electrode by the side of a substrate to the lead member, when connecting with a leadframe, the electrode by the side of a luminous layer was producing Light Emitting Diode by the method of carrying out wire bonding to other lead members. when a transparent insulation substrate is used for an element chip, in order [however,] to take the flip chip method which has the electrode of a positive/negative couple in a luminous layer side -- an element chip and a lead -- connection of a member cannot take the connection method mentioned above for this reason -- in order to connect to a leadframe two sorts of electrodes formed in the luminous layer side -- the lead of two -- the connection side with the element chip of a member is made flat, and the process which pastes up the electrode side of an element chip on this flat side with a pewter or a conductive paste is taken However, by this method, in order to have to form two sorts of electrodes in the same field, in the element chip size below 1mm angle, electrode size had the problem that two sorts of polar zone will contact in an according [if it kicks, will not become but] to pewter or conductive paste adhesion [carry out] process, with 200 micrometers or less. Moreover, the electrode area pasted up with the pewter or the conductive paste to an element chip size was not able to form a complicated electrode pattern like the shape of the shape of MIANDA used a latus sake in order to make light emit more efficiently, the letter of a network, or Cush. Or when producing the multicolor light emitting diode which obtains luminescence of two or more colors from one Light Emitting Diode, since three or more polar zone was needed, electrode area had to be made still smaller, and the connection with the electrode and lead member by the pewter or the conductive paste was impossible. Moreover, the light-emitting-device chip used for Light Emitting Diode by which the conventional proposal is made was using the transparent insulating substrate, and since there was the absorption of light by the substrate for the structure which takes out the light which emitted light through a substrate, there was also a trouble that luminous efficiency fell.
[0004] this invention tends to solve the aforementioned trouble and tends to offer Light Emitting Diode with a good luminescence property with sufficient reappearance simply.
[0005]
[Means for Solving the Problem] This invention persons can obtain now Light Emitting Diode which has a good property with sufficient reappearance by using the wire-bonding method, in case all the electrodes and each lead member of the element chip using the insulating substrate are connected, as a result of repeating research wholeheartedly, in order to solve the aforementioned trouble.
[0006] That is, this invention offers the light emitting diode characterized by the structure where all connections between an electrode and a lead member are wires in the element chip of the planar structure which has an electrode for having at least one luminous layer which consists of two or more sorts of combination chosen from the n-type-semiconductor layer, p type, and the i-type-semiconductor layer on the insulating substrate, and impressing voltage to the predetermined part of a semiconductor layer at a luminous layer.
[0007] If the front face is flat as an insulating substrate in this invention, it is good, and transparence is sufficient, and it is good even when it is opaque. As a thing typical as an insulating substrate, there are sapphire (aluminum 2O3), quartz (SiO2), magnesium-oxide (MgO), strontium-titanate (SrTiO3), calcium-fluoride (CaF2), and magnesium fluoride (MgF2), titanium oxide (TiO2), etc. however, it is good to use **'s whose lattice constant of the semiconductor thin film directly formed on a substrate suited to the lattice constant of this insulating substrate as much as possible As for the grid mismatching with the semiconductor thin film directly formed on this insulating substrate and a substrate, it is good that considering as 10% or less considers as 5% or less desirable still more preferably. For this reason, it is also desirable to use that in which only the predetermined angle turned off this transparent insulation substrate. For example, in GaN, it becomes

what has desirable using the substrate which turned off the Rth page of 9.2 degrees of sapphire. Moreover, when the grid mismatching of an insulating substrate and a semiconductor thin film is very large, you may prepare a buffer layer between this insulating substrate and a semiconductor thin film. As a buffer layer, the amorphous-like matter, for example, AlN, GaN, Si, SiC, etc., can prepare AlN, ZnO, SiC, etc. as single crystal matter.

[0008] As a method of forming a luminous layer on an insulating substrate in this invention, semiconductor growth equipments, such as the MBE (Molecular Beam Epitaxy) method, the CBE (ChemicalBeam Epitaxy) method, the MOMBE (Metal Organic MBE) method, the CVD (Chemical Vapour Deposition) method, and the MOCVD (Metal Organic CVD) method, can be used. A luminous layer is formed on an insulating substrate by the above-mentioned thin film production method. This luminous layer may be any of MIS structure, the single hetero structure of having pn junction and double hetero structure, quantum well structure, or a superstructure.

[0009] The luminous layer in this invention is a luminous layer which consists of two or more sorts of combination chosen from the n-type-semiconductor layer, p type, and the i-type-semiconductor layer. Moreover, although either a III-V group compound semiconductor or an II-VI group compound semiconductor is OK as the semiconductor which forms these luminous layers, the GaN system semiconductor which is a III-V group compound semiconductor is [that growth of a crystalline good thin film is possible, and] especially desirable to the sapphire which is an insulating substrate, CaF2, MgO, etc.

[0010] The light-emitting-device chip in this invention needs to form the electrode of a positive/negative couple in the same flat surface by the side of a luminous layer, in order to use an insulating substrate, and it must etch a luminous layer. As the etching method performed to the well of this light-emitting-device chip production, you may use whichever of the wet etching method and the dry etching method according to the kind of luminous layer. Heat-treating after etching is also desirable, by performing this heat treatment, membraneous degradation received by etching can be recovered, an interfacial resistance can be lowered, and current required for luminescence can be acquired by the low battery. What is necessary is just the furnace which can control the atmosphere of a tubular furnace, a lamp annealing furnace, etc. as equipment which heat-treats.

[0011] As the electrode formation method of the light-emitting-device chip in this invention, the MBE method, a vacuum deposition method, an electron-beam-evaporation method, a spatter, etc. occur. That from which ohmic contact is obtained by a n-type semiconductor, p type, or each i type semiconductor as an electrode material may be desirable, and a metal simple substance is sufficient as it, and it may use what mixed and alloyed two or more sorts of metals. The conditions for obtaining this ohmic contact have the good metal which has a work function smaller than the work function of a semiconductor as an electrode by the side of a n-type semiconductor, and it is good to use the metal which has a bigger work function as an electrode by the side of a p type semiconductor than the work function of a semiconductor. For example, in GaN which is a III-V group compound semiconductor, it is good for an n type GaN layer to use aluminum, In, Ti, Pb, Sb, Nb, Zr, Mn, etc. for an electrode, and good ohmic contact is obtained by i type or the p type GaN layer by using Au, Pt, germanium, As, Ir, Re, Rh, Pd, nickel, W, etc. for an electrode. Moreover, in order to raise an adhesive property, and to improve the thermal resistance of the polar zone, it is [be / in case / an element chip is pasted up on a lead member after this ohmic electrode formation,] also desirable to carry out the laminating of the metals, such as nickel, Ti, Au, and W, on an ohmic electrode.

[0012] It is also desirable to heat-treat below by the decomposition temperature of a semiconductor in the gas stream which contains the composition element of the inside of inert gas styles, such as Ar, N2, and helium, or this semiconductor after electrode formation, this is enabled to lower the interfacial resistance of an electrode and a semiconductor, and it can obtain good diode characteristics. As for Light Emitting Diode in this invention, it is desirable to devise an electrode configuration in order to take the structure which takes out light from an electrode side. In order to take out the light which emitted light from an electrode side, it is that wrap electrode area makes preferably the front face of this p type or a i-type-semiconductor layer 30% or less still more preferably 40% or less 50% or less. Therefore, although an electrode needs to form a pattern on the front face of p type or a i-type-semiconductor layer, and it can consider as the letter of a network shown in drawing 4 as an example of a pattern, the shape of Cush which are shown in drawing 5 , and the shape of MIANDA which are shown in drawing 6 , and there are combination of these patterns, the shape of a whirl and an island, etc. further, it is not limited to especially these. If the width of face of an electrode and an inter-electrode distance narrow width of face of an electrode and inter-electrode distance is made small that what is necessary is just to change with the electric resistance of p type or a i-type-semiconductor layer, or the size of voltage to impress, its ejection efficiency of light will improve. While impressing voltage to the front face of p type or a i-type-semiconductor layer uniformly by making width of face of an electrode into a submicron grade, and making inter-electrode into the interval about submicron one, ejection efficiency of light can also be enlarged.

[0013] Moreover, in this invention, it will also become desirable to prepare at least a kind of metallic reflective layer as shown on the field in which the luminous layer on a substrate is not formed at drawing 11 . It is enabled for this metal layer to reflect the light which emits light in the luminous layer which comes to combine a n-type-semiconductor layer and p type, or a i-type-semiconductor layer, and comes out through a substrate, and to take it out from an electrode side. Thereby, the ejection efficiency of the light of a light emitting device can be raised. As a material used as a metallic reflective layer, there are metaled simple substances or those alloys, such as aluminum, In, Cu, Ag, Pt, Ir, Pd, Rh, W, Mo, Ti, and nickel. A metallic reflective layer becomes what has at least a monostromatic desirable [also considering as the structure which carried out the laminating of the metal of high-melting points, such as nickel, W, and Mo, in order to make the pewter-proof nature when mounting in a leadframe, and thermal resistance and bonding-proof nature improve] although it is good.

[0014] The configuration of the leadframe in this invention is [that what is necessary is just the structure where other lead members are connectable with each electrode for impressing voltage to the connection for fixing an element chip to a lead member, and each part of an element chip with a wire, respectively.] changeable with the electrode configuration of a light-emitting-device chip. Since luminescence is condensed effectively, as for a leadframe, it is desirable to establish a mirror side.

[0015] What is generally used for the lead member as a material of the adhesion at the time of performing die bonding in the light-emitting-device chip in this invention can be used. For example, Bi little to Au-Si, an Pb-Sn alloy system pewter, and this pewter, To what added metals, such as Sb, Ag, Cd, Zn, and In, and Bi, Na, To what added and alloyed Tl, Cd, Sn, Pb, etc., and In, Zn, Cd, There is a conductive paste containing metals, such as what added and alloyed Sn, Bi, etc., a thing

which added and alloyed Ag, Zn, Sn, In, etc. to Ga, and Au, aluminum, In, Ag, Ag, Au, Cu, etc. As a method of pasting up an element chip and a lead member, there is a method using conventional die bonding equipment. namely, a glue line -- this polar zone of an element chip, or a lead -- it pastes up by heating a lead member beyond the melting point of the charge of a binder, sticking this polar zone and this lead member, after forming in the adhesion side of the element chip of a member with a vacuum deposition, the applying method, or plating

[0016] Moreover, in case the polar zone and lead member of a light-emitting-device chip in this invention are wired, it is the feature to use the wire bonder method. after fixing an element chip to a lead member by the die bonding method -- wire-bonding equipment -- setting -- heating -- and -- or the polar zone and a lead member are connected by impressing an ultrasonic wave As a material of a wire used at this time, there are alloys, such as metals, such as Au, Ag, Cu, and aluminum, Au-Si, aluminum-Si, aluminum-Mg, aluminum-Si-Mg, and aluminum-nickel, and which material is used should just choose in consideration of the material of the polar zone of a light-emitting-device chip, or the workability of wirebonding. Especially, I hear that workability is good and it is desirable. [of Au or aluminum-Si] The size of a wire is usually 20-300micrometerphi that what is necessary is just to choose in consideration of the workability of size **** wirebonding of the polar zone of a light-emitting-device chip. Moreover, in order to prevent oxidization of a wire, it is also a desirable method to perform wirebonding in inert gas.

[0017] It is desirable that the light transmittance in the luminescence wavelength range of a light-emitting-device chip uses 80% or more of translucency material as a closure material in this invention. As this translucency material, an methacrylic system resin, an epoxy system resin, a polycarbonate system resin, a polystyrene system resin, and POREORE fin system resin **** can use a kind, even if there are few low melting glasses. as the closure method -- the metal mold of for example, a request configuration -- the raw material or heating melting object of such translucency material -- a notes form -- carrying out -- metal mold -- the method of solidifying inside can be used As the method of this solidification, cooling solidification, a chemical reaction, etc. can be mentioned with the polymerization solidification by the heat or light of a monomer or oligomer, and a heating melting object. If there is need in this translucency material, it is also possible to add the lubricant for the antioxidant for stabilization of the coloring matter for color tone adjustment or visibility amendment, a pigment, a fluorescent substance, etc. of a resin, a stabilizer, and a fabricating operation and lubricant.

[0018] Although the example of Light Emitting Diode produced using the all directions method explained above is shown in drawing 3 , it is not limited to this. The element chip 24 is an element chip of the planar structure which has an electrode for having at least one luminous layer which consists of two or more sorts of combination chosen from the n-type semiconductor layer, p type, and the i type semiconductor on the insulating substrate, and impressing voltage to the predetermined part of each semiconductor layer at a luminous layer. the substrate side of this element chip, or a lead -- the lead after depositing a pewter by the vacuum deposition to the adhesion side of a member 22 -- the element chip 24 is put on the adhesion side of a member 22, and it heats beyond the melting point of a pewter and pastes up Then, each electrode and each lead member are connected by the gold streak using the wirebonding method. Then, it closes by translucency material and Light Emitting Diode25 is produced.

[0019] It is aluminum 2O3 as an insulating substrate as the following and an example. Although how to use it, form a GaN thin film using the MBE method, and produce Light Emitting Diode is explained, it is not limited to especially this. The gas source MBE equipment equipped with the crucibles 2, 3, and 4 for evaporation (Knudsen Cell), the gas cell 7, and the substrate heating electrode holder 5 in the vacuum housing 1 as shown in drawing 1 as equipment was used.

[0020] Ga metal was put into the crucible 2 for evaporation, and it heated to the temperature set to 1013-1019-/cm2 and sec in a substrate side. It was made to spray ammonia on introduction of ammonia directly from the inside of a gas cell 7 at a substrate 6 using the gas introduction pipe 8. The amount of introduction of ammonia was supplied so that it might be set to 1016-1020-/cm2 and sec in a substrate front face. In, aluminum, etc. are put into the crucible 3 for evaporation, and membranes are formed by controlling temperature and time so that it may become the semiconductor which has the compound semiconductor and the predetermined carrier density of predetermined composition. Mg, Zn, Be, Sb, Si, germanium, C, Sn, Hg, As, P, etc. are put into the crucible 4 for evaporation, it dopes by controlling temperature and supply time so that it may become the predetermined amount of supply, and n type and i type, or a p type semiconductor layer is formed.

[0021] The Rth page of sapphire was used for the substrate 6, and it heated at 200-900 degrees C. The thing of 0.8 or less degrees has [the Rth page substrate of sapphire] a desirable OFF angle. First, after heating a substrate 6 at 750 degrees C within a vacuum housing 1, each crucible is set as predetermined growth temperature, the crucible 3 for evaporation is opened first, and an n type GaN thin film with a thickness of 0.05-2 micrometers is produced by the growth rate of 0.1-30A / sec. Furthermore, after that, the shutter of the crucible 4 for evaporation which charged Zn is opened, i type or a p type GaN thin film is formed by the thickness of 0.01-1 micrometer by the growth rate of 0.1-30A / sec, and a luminous layer is formed. At the time of this membrane formation, a gas cell is always heated, and ammonia is supplied to a substrate front face.

[0022] The process which produces Light Emitting Diode using the GaN thin film which has the luminous layer which formed membranes by the above methods is explained according to drawing 2 (h) from drawing 2 (a). A vacuum deposition method is used and it is aluminum 2O3. The vacuum evaporationo of the metallic-reflection film 17 is carried out to a side (a). A resist is applied to a GaN thin film front face. As for the thickness of a resist, it is desirable to be referred to as 0.1-3 micrometers that what is necessary is just to change with the thickness of a GaN thin film to **********. The conditions of a spin coater are 2500rpm and 30sec. A prebake is carried out for 30 minutes within the clean oven heated by 90 degrees C after the application (b). Then, UV exposure and development were performed using the mask for element pattern formation (c). The GaN thin film 14 of i layers or p layers is removed by the ion milling method, using Ar as gas (d). A resist is removed after an ion milling end using an acetone.

[0023] In addition, it can decide on time to perform ion milling in each process by the thickness which etches. The sample was set after the above process and in the tubular furnace, and it heat-treated for 30 minutes at 500 degrees C by making ammonia into atmosphere. After having applied the resist again, having performed the prebake after heat treatment, and performing UV exposure and development using the mask for n layer electrode formation continuously, the vacuum evaporationo of the aluminum was carried out to the thickness of 3000A as an electrode of the n type GaN layer 15 by (e) and the vacuum deposition method, and the electrode pattern 19 was formed by the lift off (f). Subsequently, after having applied the resist again, performing the prebake and performing UV exposure and development using the mask for i layer electrode formation, the vacuum evaporationo of the Au was carried out to the thickness of 3000A as an electrode of p

type or the i type GaN layer 14 by (g) and the vacuum deposition method, and the electrode pattern 20 was formed by the lift off (h). Then, 300 degrees C and heat-treatment of 1 hour were performed in Ar style.
[0024] the metallic-reflection film of the light-emitting-device chip produced as mentioned above -- a pewter -- a lead -- a member 22 -- pasting up -- the electrode of an n type GaN layer and an i type GaN layer -- wire bonder equipment -- using -- 30micrometerphiAu lines 23 -- respectively -- a lead -- a member 21 and a lead -- bonding was carried out to the member 22 Then, 5mmphiLight Emitting Diodes25 as perform molding by the transparent epoxy resin and show a light-emitting-device chip to drawing 3 were produced.
[0025]
[Example] Hereafter, an example explains to a detail further.
[0026]
[Example 1] aluminum2 O3 R page is used as an insulating substrate, a GaN thin film is formed by the MBE method, and the example which produced Light Emitting Diode using the element chip which has MIANDA-like electrode structure is explained. The MBE equipment equipped with the crucibles 2 and 4 for evaporation, the gas cell 7 and the substrate heating electrode holder 5, and the gas introduction pipe 8 for supplying gas to a gas cell 7 further in the vacuum housing 1 as shown in drawing 1 was used.
[0027] Ga metal was put into the crucible 2 for evaporation, and it heated at 1050 degrees C. Ammonia was used as gas and the gas cell 7 was supplied at the rate of 5 cc/min through the gas introduction pipe 8. Ammonia gas was made into structure which is directly supplied to a substrate 6. As a substrate 6, an OFF angle uses the Rth page of the sapphire which is 0.5 degrees. The pressure in a vacuum housing was 2x10-6Torr at the time of membrane formation.
[0028] First, it heats for 30 minutes at 900 degrees C, and membranes are formed by subsequently to the temperature of 750 degrees C holding a substrate 6. Membrane formation is performed by opening the shutter of the crucible of Ga, supplying ammonia from the gas cell 7 heated at 300 degrees C, and it is 0.5 micrometers of thickness at 1.5A / membrane formation speed of sec. The n type GaN thin film was produced. The shutter of the crucible 4 for evaporation which furthermore charged Mg and was kept at 300 degrees C was opened, the GaN thin film of Mg dope was formed by the thickness of 0.05 micrometers of thickness at 1.5A / membrane formation speed of sec, and the luminous layer was formed. Crystallinity and flat nature were good at the shape of a streak, and when the RHEED pattern of this produced thin film measured resistance, it had resistance of 10 M omega or more, and was in the insulating state.
[0029] The vacuum deposition method was used for the opposite side of the substrate side in which the luminous layer is formed, the vacuum evaporationo of the aluminum was carried out to it by the thickness of 3000A in the vacuum of 2x10-6Torr, and the reflective film was formed in it. Then, on the luminous layer, the spin coater was used, the resist was applied on condition that 2500rpm and 30sec, and the prebake was carried out for 30 minutes in 90-degree C clean oven. After BEKU, using the mask for element pattern formation, UV exposure was carried out and negatives were developed. Then, ion milling was performed for 15 minutes by Ar of the conditions of acceleration voltage 500V and pressure 2x10-4Torr, and element pattern formation was performed. Then, the resist was removed using the acetone. Next, the resist was again applied on condition that 2500rpm and 30sec using the spin coater, and the prebake was carried out for 30 minutes in 90-degree C clean oven. After BEKU, using the mask for i layer removal, UV exposure was carried out and negatives were developed. Then, ion milling was performed for 1 minute in Ar atmosphere of the conditions of acceleration voltage 500V and pressure 2x10-4Torr, and i unnecessary layers were removed. Then, the acetone removed the resist. Subsequently, it set to the tubular furnace and 500 degrees C and heat treatment for 30 minutes were performed in the ammonia gas stream of 10 cc/min. Furthermore, the resist was applied on condition that 2500rpm and 30sec using the spin coater, and the prebake was carried out for 30 minutes in 90-degree C clean oven. After BEKU, using the mask for electrode formation of an n type GaN layer, UV exposure was carried out and negatives were developed. Then, the vacuum deposition machine was equipped and vacuum deposition of the aluminum metal was carried out by the thickness of 0.2 micrometers in the vacuum of 2x10-6Torr. Then, the lift off was carried out with the acetone and the electrode pattern was formed. Subsequently, using the mask for electrode formation of an i type GaN layer, UV exposure was carried out and negatives were developed. Then, the vacuum deposition machine was equipped and vacuum deposition of the Au metal was carried out by the thickness of 0.2 micrometers in the vacuum of 2x10-6Torr. Then, the lift off was carried out with the acetone and the electrode pattern was formed. Heat-treatment was performed for this produced light emitting device at 300 degrees C in Ar style for 1 hour, and the element chip which has MIANDA-like electrode structure was completed. The side elevation and plan of an element chip which were produced were shown in drawing 7 (a) and (b).
[0030] Cutting of each chip was performed using the dicing saw. The one-element chip was set to 0.5mmx0.5mm. One chip of these was taken out and die bonding of the reflective film side was carried out to the lead member with Ag paste. Furthermore, an n type GaN layer electrode, an i type GaN layer electrode, and each lead member were connected by 30micrometerphiAu lines using wire-bonding equipment. Light Emitting Diode as closed the light emitting device produced by the above-mentioned method by the transparent epoxy resin and shown in drawing 8 was produced.
[0031] When 100 Light Emitting Diodes were produced by the same method, luminescence was checked by 99 Light Emitting Diodes. When the luminescence intensity of this Light Emitting Diode is measured, it is 60mcd(s) in 8V and 20mA, and blue luminescence was observed.
[0032]
[The example 1 of comparison] It is aluminum 2O3 by the same method as an example 1. Element-ization was performed using the GaN thin film which has the luminous layer which formed membranes on the substrate. Element production process was also performed by the same method as an example 1, and with Ag paste, after the two electrodes of an n type GaN layer and an i type GaN layer performed die bonding to the lead member, they were closed by the transparent epoxy resin and produced Light Emitting Diode. When 100 Light Emitting Diodes were produced by the same method, the electrode of positive/negative was connected with Ag paste and what emits light only by nine Light Emitting Diodes was not obtained.
[0033]
[Example 2] aluminum2 O3 R page is used as an insulating substrate, and the example which formed the Ga1-x Inx N thin film by the MBE method, and produced Light Emitting Diode of 2 color luminescence is explained. The MBE equipment equipped with the crucibles 2, 3, and 4 for evaporation, the gas cell 7 and the substrate heating electrode holder 5, and the gas introduction pipe 8 for supplying gas to a gas cell 7 further in the vacuum housing 1 as shown in drawing 2 was used.
[0034] Ga metal was put into the crucible 2 for evaporation, and it heated at 1020 degrees C, and In metal was put into the

crucible 3 for vacuum evaporationo, and it heated at 1000 degrees C. Ammonia was used as gas and the gas cell 7 was supplied at the rate of 5 cc/min through the gas introduction pipe 8. Ammonia gas was made into structure which is directly supplied to a substrate 6. As a substrate 6, an OFF angle uses the Rth page of the sapphire which is 0.5 degrees.
[0035] The pressure in a vacuum housing was 2x10-6Torr at the time of membrane formation. First, it heats for 30 minutes at 900 degrees C, and membranes are formed by subsequently to the temperature of 700 degrees C holding a substrate 6. Membrane formation is performed by opening the shutter of the crucible of Ga and In, supplying ammonia from the gas cell 7 heated at 300 degrees C, and it is 0.5 micrometers of thickness at 1.5A / membrane formation speed of sec. The n type Ga0.8 In0.2 N thin film was produced. The i type Ga0.8 In0.2 N thin film which opened the shutter of the crucible 4 for evaporation which furthermore charged Mg and was kept at 300 degrees C, and doped Mg was formed by the thickness of 0.05 micrometers of thickness at 1.5A / membrane formation speed of sec, and the 1st luminous layer was formed. Next, after raising substrate temperature to 750 degrees C and stabilizing temperature for 30 minutes, open the shutter of the crucible of Ga and the n type GaN thin film of 0.5 micrometers of thickness is grown up by the growth rate of 1.5A / sec. The i type GaN thin film which furthermore opened the shutter of the vacuum evaporationo crucibles 2 and 4 on it, and doped Mg was formed by the thickness of 0.05 micrometers of thickness by the growth rate of 1.5A / sec, and the 2nd luminous layer was formed.
[0036] The vacuum deposition method was used for the opposite side of the substrate side in which the luminous layer is formed, the vacuum evaporationo of the aluminum was carried out to it by the thickness of 3000A in the vacuum of 2x10-6Torr, and the reflective film was formed in it. Then, on the luminous layer, the spin coater was used, the resist was applied on condition that 2500rpm and 30sec, and the prebake was carried out for 30 minutes in 90-degree C clean oven. After BEKU, using the mask for element pattern formation, UV exposure was carried out and negatives were developed. Then, ion milling was performed for 25 minutes by Ar of the conditions of acceleration voltage 500V and pressure 2x10-4Torr, and element pattern formation was performed. Then, the resist was removed using the acetone. Next, the resist was again applied on condition that 2500rpm and 30sec using the spin coater, and the prebake was carried out for 30 minutes in 90-degree C clean oven. After BEKU, using the photo mask, UV exposure was carried out and negatives were developed. Then, ion milling was performed for 15 minutes in Ar atmosphere of the conditions of acceleration voltage 500V and pressure 2x10-4Torr, and the unnecessary i type GaN layer, the n type GaN layer, and the i mold Ga0.8 In0.2 N layer were removed. Next, the resist was again applied on condition that 2500rpm and 30sec using the spin coater, and the prebake was carried out for 30 minutes in 90-degree C clean oven. After BEKU, using the photo mask, UV exposure was carried out and negatives were developed. Subsequently, ion milling was performed for 13 minutes in Ar atmosphere of the conditions of acceleration voltage 500V and pressure 2x10-4Torr, and the unnecessary i type GaN layer and the n type GaN layer were removed. The resist was applied on condition that 2500rpm and 30sec using the spin coater further again, and the prebake was carried out for 30 minutes in 90-degree C clean oven. After BEKU, using the photo mask, UV exposure was carried out and negatives were developed. Then, the unnecessary i type GaN layer was removed using ion milling. Then, the acetone removed the resist. Subsequently, it set to the tubular furnace and 500 degrees C and heat treatment for 30 minutes were performed in the ammonia gas stream of 10 cc/min. Furthermore, the resist was applied on condition that 2500rpm and 30sec using the spin coater, and the prebake was carried out for 30 minutes in 90-degree C clean oven. After BEKU, using the mask for electrode formation of an n type GaN layer and n mold Ga0.8 In0.2 N layer, UV exposure was carried out and negatives were developed. Then, the vacuum deposition machine was equipped and vacuum deposition of the aluminum metal was carried out by the thickness of 0.2 micrometers in the vacuum of 2x10-6Torr. Then, the lift off was carried out with the acetone and the electrode pattern was formed. Subsequently, using the mask for electrode formation of an i type GaN layer and i mold Ga0.8 In0.2 N layer, UV exposure was carried out and negatives were developed. Then, the vacuum deposition machine was equipped and vacuum deposition of the Au metal was carried out by the thickness of 0.2 micrometers in the vacuum of 2x10-6Torr. Then, the lift off was carried out with the acetone and the electrode pattern was formed. Heat-treatment was performed for this produced light emitting device at 300 degrees C in Ar style for 1 hour, and the structure of an element chip was completed. The side elevation and plan of an element chip which were produced are shown in drawing 9 (a) and (b).
[0037] Cutting of each chip was performed using the dicing saw. The one-element chip was set to 1mmx1mm. One chip of these was taken out and die bonding of the reflective film side was carried out to the lead member with the Pb-Sn pewter. The n type GaN layer and the n mold Ga0.8 In0.2 N layer electrode were connected by 30micrometerphiAu lines using wire-bonding equipment after that. Furthermore, the i type GaN layer electrode, a lead member and an i type Ga0.8 In0.2 N layer electrode, and the lead member were connected by 30micrometerphiAu lines using wire-bonding equipment. The light emitting device produced by the above-mentioned method was closed by the transparent epoxy resin, and Light Emitting Diode as shown in drawing 10 was produced.
[0038] When 100 Light Emitting Diodes were produced by the same method, luminescence was checked by 95 Light Emitting Diodes. the place which measured the luminescence intensity of this Light Emitting Diode -- a lead -- a member 66 and a lead -- a member 67 -- 10V and luminescence with blue 40mcd(s) at 18mA -- a lead -- a member 66 and a lead -- in the member 68, 8V and luminescence with green 60mcd(s) at 20mA were observed
[0039]
[Effect of the Invention] this invention is connecting respectively all the electrodes formed in the same flat surface to the lead member divided into the same number as this number of electrodes with a wire by the wire-bonding method in the planar type element chip structure the luminous layer's having been formed on the insulating substrate, and it becomes possible to supply Light Emitting Diode of the stable performance.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the schematic diagram of the MBE equipment used for thin film production.
[Drawing 2] (a) - (h) It is the cross section having shown the production process of Light Emitting Diode.
[Drawing 3] It is the cross section of Light Emitting Diode produced by the method by this invention.
[Drawing 4] It is the plan of the light emitting device in which the letter electrode of a network was formed.
[Drawing 5] It is the plan of the light emitting device in which the Cush-like electrode was formed.
[Drawing 6] It is the plan of the light emitting device in which the MIANDA-like electrode was formed.
[Drawing 7] (a) It is the cross section of the element chip produced in the example 1.
(b) It is the plan of the element chip produced in the example 1.
[Drawing 8] It is the cross section of Light Emitting Diode produced in the example 1.
[Drawing 9] (a) It is the cross section of the element chip produced in the example 2.
(b) It is the plan of the element chip produced in the example 2.
[Drawing 10] It is the cross section of Light Emitting Diode produced in the example 2.
[Drawing 11] It is the cross section of a light emitting device which consists of structure where the metal layer was formed in the near substrate side in which a luminous layer is not formed.
[Drawing 12] It is the cross section of Light Emitting Diode produced by the conventional method.
[Drawing 13] It is the cross section of Light Emitting Diode of the flip chip method produced by the conventional method.
[Description of Notations]
1 Vacuum Housing
2 Crucible for Evaporation
3 Crucible for Evaporation
4 Crucible for Evaporation
5 Substrate Heating Electrode Holder
6 Substrate
7 Gas Cell
8 Gas Introduction Pipe
9 Flow Regulation Bulb
10 Cryopanel
11 Cold Trap
12 Oil Diffusion Pump
13 Oil Sealed Rotary Pump
14 P Type or I-Type-Semiconductor Layer
15 N-type-Semiconductor Layer
16 Insulating Substrate
17 Metallic-Reflection Film
18 Resist
19 N-type-Semiconductor Layer Electrode
20 P Type or I-Type-Semiconductor Layer Electrode
21 Lead Member (1)
22 Lead Member (2)
23 Metal Wire
24 Element Chip
25 LED
26 Electrode
27 I Type GaN Layer Electrode
28 N Type GaN Layer Electrode
29 I Type GaN Layer
30 N Type GaN Layer
31 Silicon on Sapphire
32 Aluminum Reflective Film
33 Lead Member (3)
34 Lead Member (4)
35 Au Wire
36 GaN Light-Emitting-Device Chip
37 GaNMIS Type Light Emitting Diode
38 I Type Ga0.8 In0.2 N Layer Electrode
39 N Type GaN Layer and N Type Ga0.8 In0.2 N Layer Electrode
40 I Mold Ga0.8 In0.2 N Layer
41 N Mold Ga0.8 In0.2 N Layer
42 Lead Member (5)
43 Lead Member (6)

44 Lead Member (7)
45 GaN, Ga0.8 In0.2 N Light-Emitting-Device Chip
46 2 Color Luminescence Light Emitting Diode
47 Lead Member (8)
48 Lead Member (9)
49 Leadframe
50 Mirror Side
51 Lead Member (10)
52 Lead Member (11)

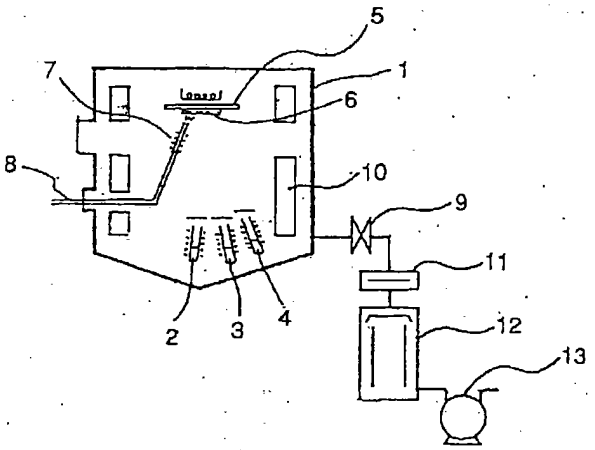
[Translation done.]

* NOTICES *

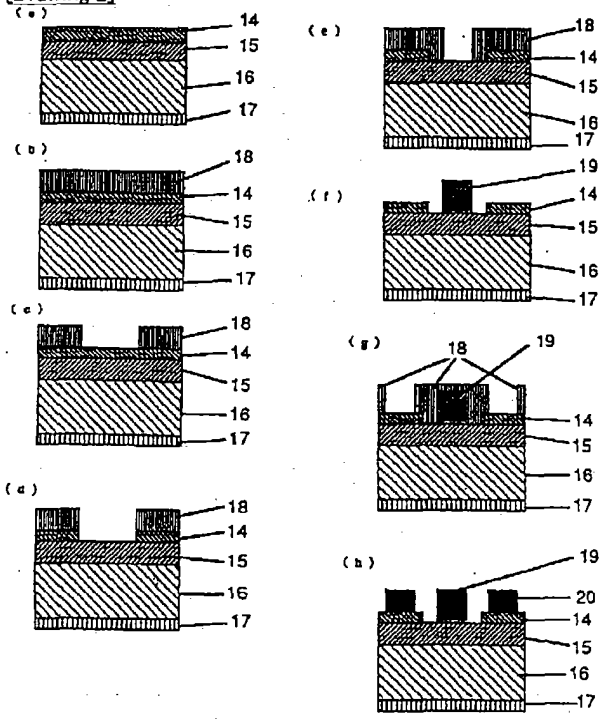
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

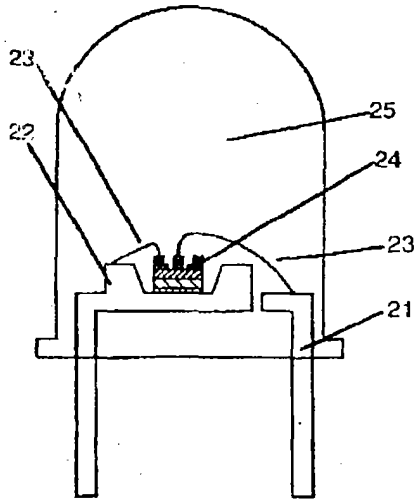
[Drawing 1]



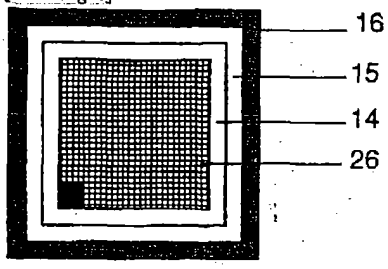
[Drawing 2]



[Drawing 3]



[Drawing 4]



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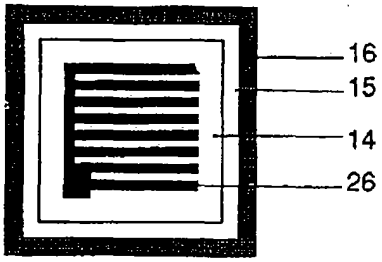

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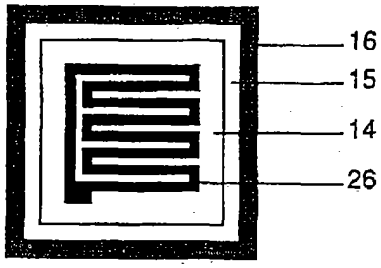

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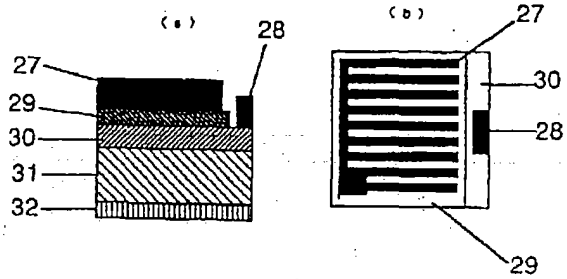
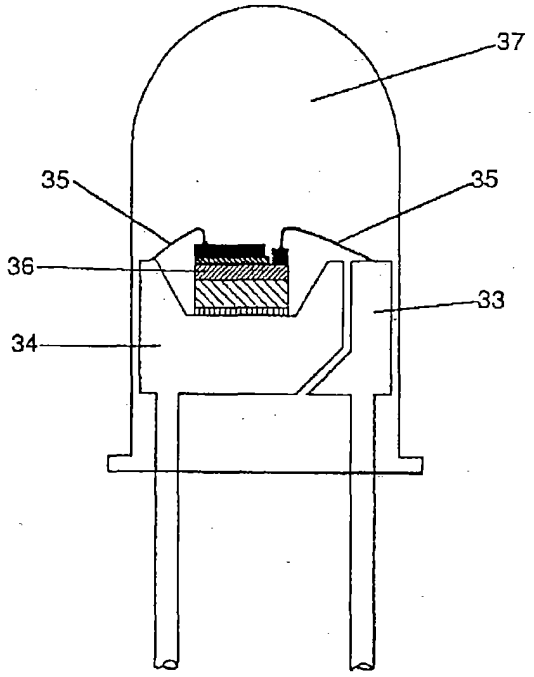
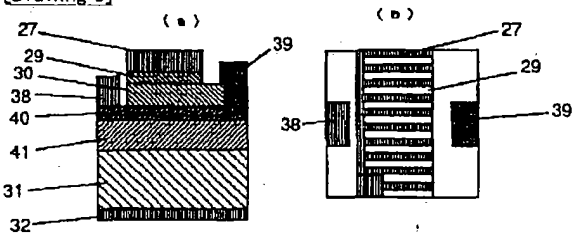


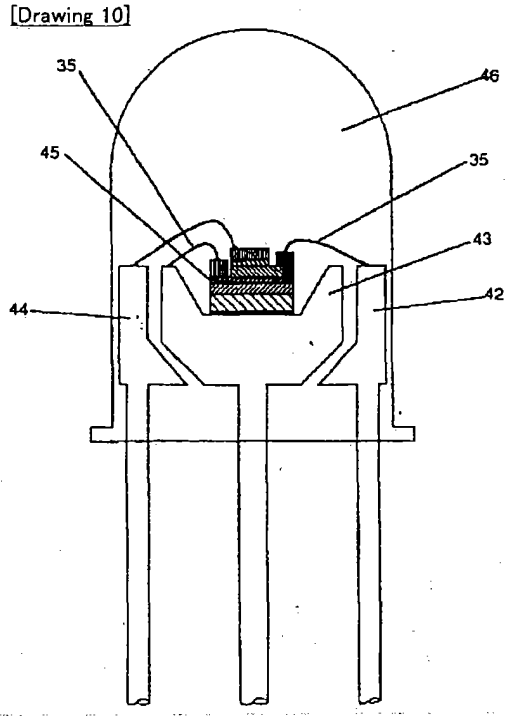
[Drawing 8]



[Drawing 9]



[Drawing 10]



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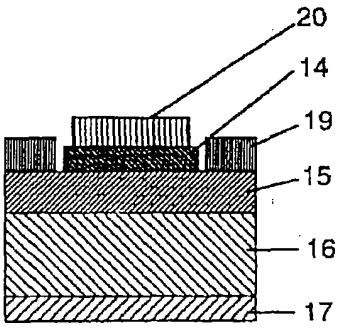
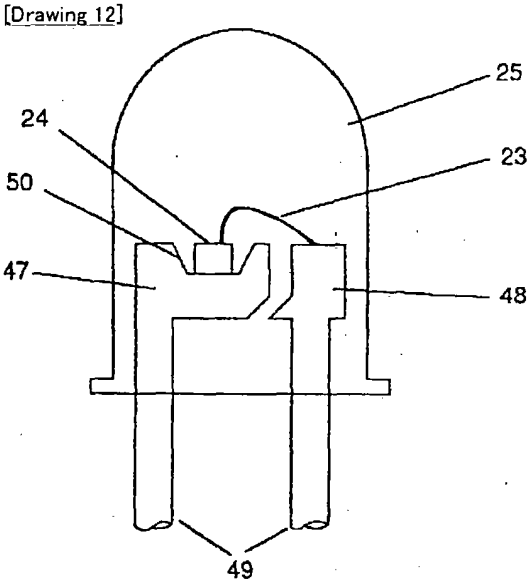
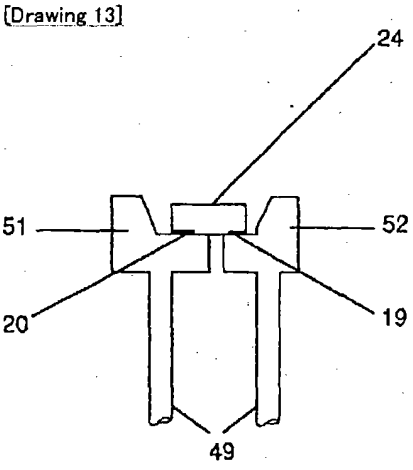


[Drawing 12]



[Drawing 13]



[Translation done.]